AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-6. (*Cancelled*).

7. (*Currently Amended*) A clock control circuit comprising:

a stage to which a plurality of clocks of mutually different phases are input, this stage generating a plurality of control signals corresponding to transition timing of one clock of the plurality of clocks and to phase differences between the clocks;

a switch group, whose switching is controlled by the control signals, for controlling charging and discharging of a capacitor, wherein the phase differences between the clocks vary the charging or discharging speed of the capacitor by shifting the switch control timings of switches in the switch group; and

a stage of converting terminal voltage of the capacitor to a logic signal and outputting the logic signal~~; and~~

~~a stage of varying charging or discharging speed of the capacitor by shifting switching control timings of switches in said switch group~~.

8-59. (*Cancelled*).